We claim:

1. A non-volatile semiconductor memory comprising:

an array of memory cells;

drivers and decoders coupled to apply voltages to the array to read any memory cell in the array, wherein each memory cell that stores data has a threshold voltage that identifies a multibit data value written in the memory cell;

an error detection circuit that detects errors in threshold voltages of memory cells storing data, wherein in response to detecting an error in the threshold voltage of a memory cell, the error detection circuit signals for a refresh operation; and

a control circuit coupled to control the drivers and decoders, wherein during the refresh operation, the control circuit writes a corrected threshold voltage that corrects the error that the error detection circuit detected.

2. The memory of claim 1, wherein the control circuit writes the correct threshold voltage to the memory cell in which the error detection circuit detected the error.

3. The memory of claim 1, wherein the control circuit writes the correct threshold voltage to a memory cell other than the memory cell in which the error detection circuit detected the error.

4. The memory of claim 3, further comprising an address mapping circuit that accounts for an address mapping, wherein when the control circuit writes the corrected threshold voltage to the other memory cell, the address mapping circuit changes the address mapping to indicate a new physical location for the correct threshold voltage.

5. The memory of claim 1, wherein the control circuit reads refresh information for a sector containing the memory cell having the error in the threshold voltage and based on the refresh information selects where to write the

corrected threshold voltage.

6. The memory of claim 1, wherein the control circuit reads a count of erase cycles for a sector containing the memory cell having the error in the threshold voltage and based on the count selects where to write the corrected threshold voltage.

7. The non-volatile memory of claim 1, wherein the error detection circuit comprises:

a reference generator that generates first reference signals and second reference signals, the first reference signals indicating bounds of ranges of threshold voltages allowed for the memory cells storing data, and the second reference signals indicating bounds of one or more ranges of threshold voltages forbidden for the memory cells storing data; and

a circuit that determines whether a threshold voltage of a memory cell is in one of the ranges allowed or one of the ranges forbidden.

8. The non-volatile memory of claim 1, wherein the error detection circuit processes an error detection code to identify a data error in data read from the array, the data error indicating the threshold voltage error in the memory cell.

9. The non-volatile memory of claim 1 further comprising a data correction circuit that processes an error correction code to identify the corrected threshold voltage.

10. A non-volatile semiconductor memory comprising:

an array of memory cells;

drivers and decoders coupled to apply voltages to the array to read any memory cell in the array, wherein each memory cell that stores data has a threshold voltage that identifies a multibit data value written in the memory cell;

a reference generator that generates first reference signals and second reference signals, wherein the first reference signals indicate bounds of ranges of threshold voltages allowed for the memory cells storing data, and the second reference signals indicate bounds of one or more ranges of threshold voltages forbidden for the memory cells storing data; and

a control circuit coupled to control the drivers and decoders during a refresh operation that reads a threshold voltage of a memory cell, detects whether the threshold voltage of the memory cell is in a range forbidden for memory cells storing data, and moves the threshold voltage of the memory cell into one of the ranges allowed for memory cells storing data.

11. The non-volatile memory of claim 10, further comprising a timer that periodically triggers the control circuit to start the refresh operation for at least a portion of the memory array.

12. The non-volatile memory of claim 11, wherein the array, the drivers and decoders, the reference generator, the control circuit, and the timer are parts of a monolithic integrated circuit.

13. The non-volatile memory of claim 11, further comprising a buffer coupled to temporarily store data from the portion of the memory array, during the refresh operation.

14. The non-volatile memory of claim 11, wherein a sector of the memory array temporarily stores data from the portion of the memory array, during the refresh operation.

15. The non-volatile memory of claim 10, wherein the ranges of threshold voltages allowed for memory cells storing data are separated from each other by at least one range of threshold voltages forbidden for memory cells storing data.

16. A non-volatile semiconductor memory comprising:

an array of memory cells;

drivers and decoders coupled to apply voltages to the array to read any memory cell in the array, wherein each memory cell that stores data has a threshold voltage that identifies a multibit data value written in the memory cell; and

a reference generator that generates signals indicate bounds of a plurality of ranges of threshold voltages allowed for the memory cells that store data, wherein each range in the plurality corresponds to a multibit value that differs in only a single bit from a multibit value corresponding to a range that is adjacent in threshold voltage.

17. The memory of claim 16, wherein the reference generator further generates reference signals indicating bounds of one or more ranges of threshold voltages forbidden for the memory cells storing data.

18. The memory of claim 17, further comprising a control circuit coupled to control the drivers and decoders, wherein during a refresh operation, the control circuit detects whether the threshold voltage of the memory cell is in a range forbidden for memory cells storing data, and sets the threshold voltage of a memory cell in the array into one of the ranges allowed for memory cells storing data.

19. The memory of claim 16, further comprising a control circuit coupled to control the drivers and decoders, wherein during a refresh operation, the control circuit detects whether data stored a memory cell contains a data error, uses a error correction code stored in the memory array to identify a correct data value for the memory cell, and sets the threshold voltage of a memory cell in the array into the range corresponding to the correct data value.

20. A method for operating a non-volatile memory, comprising:

writing a multibit digital value to a memory cell by programming a threshold voltage of the memory cell to level within a target range of threshold voltages, wherein the target range of threshold voltages is one of a plurality of first ranges of threshold voltages, each of the first ranges corresponding to a different multibit value;

measuring the threshold voltage of the memory cell;

identifying whether the threshold voltage is still in a range from the plurality of first ranges or is in a range from a second plurality of ranges of threshold voltages; and

in response to the threshold voltage being in the second plurality of threshold voltages, changing the threshold voltage so that the threshold voltage is in one of the first plurality of ranges of threshold voltages.

21. The method of claim 20, wherein changing the threshold voltage increases the threshold voltage so that the threshold voltage is in a nearest one of the first ranges.

22. The method of claim 20, wherein changing the threshold voltage decreases the threshold voltage so that the threshold voltage is in a nearest one of the first ranges.

23. The method of claim 20, wherein:

the plurality of first ranges of threshold voltages form a sequence of ranges ordered according to increasing maximum voltages;

each first range corresponds to a different multibit digital value; and

the multibit digital value for each range differs by only one bit, from the multibit value for the range immediately preceding in the series.